Sole Inventor

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Charissa Wheeler

APPLICATION FOR UNITED STATES LETTERS PATENT

SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

Be it known that I, **Sang Hun OH**, a citizen of the Republic of Korea, residing at 222 Dondang-dong, Wonmi-gu, Bucheon-si, Gyeonggi-do, Korea have invented new and useful **METHODS FOR FORMING AN AIR GAP IN A SEMICONDUCTOR METAL LINE MANUFACTURING PROCESS**, of which the following is a specification.

METHODS FOR FORMING AN AIR GAP IN A SEMICONDUCTOR METAL LINE MANUFACTURING PROCESS

FIELD OF THE DISCLOSURE

[0001] The present disclosure relates to semiconductor devices; and, more particularly, to methods for forming an air gap in a semiconductor metal line manufacturing process to manufacture a semiconductor device exhibiting low capacitance.

BACKGROUND

[0002] Recently, semiconductor devices are being manufactured such that metal lines are formed on every layer of a multi-layered structure. The distance between vertically adjacent metal lines on an upper layer and a lower layer of the multi-layered structure is getting smaller. Additionally, the gap between metal lines placed on the same layer has been narrowed. For example, the distance between horizontally adjacent metal lines located on the same layer is getting smaller. As a result of these changes, semiconductor devices have become even more highly integrated.

[0003] The small distances between vertically or horizontally adjacent metal lines considerably affects the parasitic resistance and the parasitic capacitance between the metal lines in the multi-layered structure. The parasitic resistance and the parasitic capacitance are highly likely to deteriorate electrical characteristics of the associated device, especially, a VLSI (Very Large Scaled Integration) semiconductor device. Furthermore,

the level of power consumption and the amount of signal leakage of the device may be increased due to an (RC) delay introduced by the parasitic resistance and capacitance.

[0004] Therefore, it is very important to develop a wiring technique for constructing a highly efficient multi-layered metal lines structure exhibiting a low RC value in a VLSI semiconductor device. In order to construct the highly efficient multi-layered metal lines structure, it is required to form a wiring layer by employing a metal having a low resistivity or to use an insulating film exhibiting a low permittivity.

[0005] Thus, research has been reported for reducing the capacitance of materials exhibiting low permittivities, (for example, SiO series in oxide of existing TEOS series). However, it is difficult to employ such materials in actual processing because the materials exhibiting low permittivities are not identified yet.

[0006] Alternatively, an air gap technique which serves to exhibit low permittivity in spite of applying a conventionally used material has been widely studied. Specifically, when employing air exhibiting a very low permittivity of 1, the parasitic capacitance seen at the multi-layered metal lines structure can be reduced in a VLSI semiconductor device and a low permittivity can be obtained by forming an air gap while using the existing TEOS (Tetra Ethyl Ortho Silicate) series.

[0007] However, the conventional air gap forming method has a problem in that an irregular air gap may be formed.

[0008] Referring to Fig. 1, a conventional air gap forming process in a semiconductor metal line manufacturing method is represented. A via plug 108 is formed between a lower metal line 102 and a top metal line 116. If the via plug 108 is misaligned with the lower metal line 102, a metal stringer A may remain around an air gap 114, thereby shorting the bottom and the top metal lines 102 and 116. In other words, a bad air gap may be formed because the via process is carried out after forming the air gap 114.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Fig. 1 is a cross-sectional view of a semiconductor device illustrating a conventional air gap forming process.

[0010] Figs. 2A to 2G are cross-sectional views of an example semiconductor device illustrating a sequence of example processes for forming an air gap in an example semiconductor metal line manufacturing method.

DETAILED DESCRIPTION

[0011] Figs. 2A to 2G are cross-sectional views illustrating an example sequence of processes for forming an air gap in an example semiconductor metal line manufacturing method.

[0012] In the example of Fig. 2A, a lower metal line 202 is stacked on a lower insulating layer 200, (e.g., a silicon substrate coated with an oxide thereof). An upper insulting layer 204 is laid on the lower metal line 202, and

then a first photosensitive film 206 is patterned on the upper insulating layer 204.

[0013] As shown in Figs. 2B and 2C, the upper insulating layer 204 is etched away using the patterned first photosensitive film 206 as a mask. The upper insulating layer 204 is etched away until a top surface of the lower metal line 202 is exposed. Then the first photosensitive film 206 is removed from the upper insulating layer 204. A nitride film 208 is deposited on the exposed surface of the lower metal line 202 to fill up an etched portion of the upper insulating layer 204. Thereafter, an etchback process is carried out with respect to the nitride film 208 and the upper insulating layer 204 is removed from the lower metal line 202.

[0014] Referring to Fig. 2D, a second photosensitive film 210 is patterned on the structure of Fig. 2C.

[0015] As shown in Fig. 2E, the lower metal line 202 is etched away (using the patterned second photosensitive film 210 as a mask) until a top surface of the lower insulating layer 200 is exposed. The second photosensitive film 210 is then removed. Thereafter, an IMD (Inter Metal Dielectric) layer 212 is deposited over the entire structure, thereby forming an air gap 214 within the IMD layer 212.

[0016] Referring to Fig. 2F, the IMD layer 212 is planarized by a CMP (Chemical Mechanical Polishing) process until a top surface of the nitride film 208 is exposed. Thereafter, the nitride film 208 is etched away by a wet etching, thereby forming a hole in the IMD layer 212.

[0017] Finally, as shown in Fig. 2G, the hole in the IMD layer 212 is filled with a conductive material 215 for a contact plug. Thereafter, an upper metal line 216 is deposited over the structure. Such processes can be executed by a conventional contact plug process or an Al/Cu damascene process.

[0018] An example VLSI semiconductor device constructed in accordance with the above disclosure exhibits low capacitance even if employing a conventionally used material. Further, the delay caused by the RC components can be efficiently improved by forming a stable air gap without the occurrence of metal stringers.

[0019] From the foregoing, persons of ordinary skill in the art will appreciate that the above disclosed methods are capable of forming a more stable air gap by constructing both a metal line and a via line on a single object.

[0020] For instance, an example method for forming an air gap in a semiconductor metal line manufacturing process, comprises: sequentially stacking a lower insulating layer, a lower metal line and an upper insulating layer; patterning a first photosensitive film on the upper insulating layer, etching the upper insulating layer using the patterned first photosensitive film as a mask until the upper metal line is exposed; removing the first photosensitive film, filling an etched portion of the upper insulating layer with a nitride film; removing the upper insulating layer; patterning a second photosensitive film on the resultant construct, using the second photosensitive film as a mask to etch the lower metal line until the lower insulating layer is exposed; removing the second photosensitive film; depositing an IMD (Inter

Metal Dielectric) layer over the resultant construct, thereby forming an air gap within the IMD layer; planarizing the IMD layer and etching away the nitride film, thereby forming a hole; filling the hole with a conductive material for a contact plug; and depositing an upper metal line over the resultant construct.

[0021] Although certain example methods and apparatus have been described herein, the scope of coverage of this patent is not limited thereto. On the contrary, this patent covers all methods, apparatus and articles of manufacture fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.